IN THE CLAIMS

1. (Currently Amended) An e~~E~~lectronic device containing protected data, comprising:

[[-]]memory protection logic~~means~~ operable to interface with memory for storing ~~said~~ protected data therein, wherein access to said protected data is restricted for access by a local processor for execution thereon within said device;

[[-]]~~checking means~~validation logic, operative in a first mode, for checking the validity of said data and for producing a validity signal ~~enabling~~ to determine whether said data is valid; and

[[-]]validity signal output control ~~means~~logic for inhibiting an output of said validity signal to outside said device until the validity of a predetermined quantity of said protected data has been checked.

2. (Currently Amended) The device of claim 1, wherein said validity signal output control ~~means~~logic inhibits the output of said validity signal until the validity of all said protected data has been checked.

3. (Currently Amended) The device of claim 1, further comprising means operative in said first mode for transferring said data to be checked to said ~~checking means~~validation logic by cycling through successive memory addresses.

4. (Currently Amended) The device of claim 1, wherein said ~~checking means~~validation logic performs an algorithm involving each item of said protected data to be checked and yielding said validity signal in the form of a value resulting from said algorithm.

5. The device of claim 4, wherein said algorithm IS a checksum calculation.

6. (Currently Amended) The device according to claim 1, wherein said protected data is bound by first and second extremity addresses, said device comprising mode control means authorizing access into said first mode only when said first extremity address of said memory is selected as a starting point for transferring data therefrom to said ~~checking means~~validation logic.

7. The device according to claim 6, wherein said mode control means causes an exit from said first mode after said second extremity address has been attained.

8. (Currently Amended) The device according to claim 1, wherein said validity signal output control ~~means~~logic is operative to inhibit said output of said validity signal all the while said first mode is active.

9. (Currently Amended) The device of claim 1, provided with a device reset function, wherein said device further comprises reset means for resetting said ~~checking means~~validation logic in response to a device reset in said first mode.

10. The device of claim 1, provided with a device reset function, wherein said device further comprises means for exiting from said first mode upon a device reset.

11. (Currently Amended) The device of claim 10, wherein said device reset ~~means~~function comprises latching means for temporarily latching a logic state indicating the presence of the first mode and gating means for transferring the device reset signal to a reset input of the ~~checking means~~validation logic only when said logic state is present in the latching means, the latching means temporarily maintaining said gating means enabled after a disappearance of the logic state caused by the device reset signal.

12. The device of claim 1, further comprising reset means operative to reset said validity signal upon said device being forced to leave said first mode prematurely.

13. (Currently Amended) The device of claim 1, wherein said validity signal output control ~~means~~logic comprises gating means for controllably transferring said validity signal to outside said device, said gating means having an inhibit input connected to receive a mode signal for inhibiting transfer of said validity signal all the while said first mode is active.

14. (Currently Amended) The device of claim 1, wherein said memory means comprises a chip select or chip enable input, said input being connected to selection means delivering an enable signal when a first mode selection signal, and a protection Option signal are active.

15. The device of claim 14, wherein said selection means delivers said enable signal on a further condition that an address belonging to said memory means has been selected at an address input thereof.

16. The device of claim 1, wherein at least said memory and said checking device are formed on a common chip and interconnected by an internal bus.

17. The device of claim 1, wherein said memory means is a read-only memory.

18. The device of claim 1, wherein said protected data comprises program code.

19. The device of claim 1, implemented in a microcontroller unit or microprocessor chip.

20. (Currently Amended) A method of protecting data contained in memory ~~means~~ of an electronic device, the method comprising:

coupling memory protection logic to interface with memory for storing protected data therein, wherein access to said protected data is restricted for access by a local processor for execution thereon within said device;

~~associated with~~ checking, during~~means and operative in~~ a first mode, ~~for checking~~ the validity of said data and ~~for~~ producing a validity signal indicative of whether said data is valid~~,~~;

~~said method comprising the step of~~ inhibiting an output of said validity signal to outside said device until the validity of a predetermined quantity of said protected data has been checked.

21. (Currently Amended) The method of claim 20, wherein said validity signal output control means inhibits the output of said validity signal until the validity of all said data to be protected has been checked.

22. The method of claim 20, wherein said data to be checked is ~~transferred to said~~ check~~inged means~~ by cycling through successive memory addresses.

23. The method of claim 20, wherein said check involves performing an algorithm on each item of said protected data to be checked and yielding said validity signal in the form of a value resulting from said algorithm.

24. The method of claim 23, wherein said algorithm is a checksum calculation.

25. The method of claim 20, wherein said protected data is bound by first and second extremity addresses, and access into said first mode is authorized only when said first extremity address of said memory is selected as a starting point for transferring data therefrom to said checking ~~means~~.

26. (Currently Amended) The method according to claim 25, ~~further comprising the step of from~~ wherein said access into said first mode is authorized only when said first extremity address along with ~~when~~ said second extremity address has been selected.

27. The method according to claim 20, wherein said output of validity signal is inhibited all the while said first mode is active.

28. (Currently Amended) The method of claim 20, further comprising the step of resetting a validity signal in response to a device reset in said first mode.

29. The method of claim 20, further comprising the step of exiting from said first mode upon a device reset.

30. The method of claim 29, further comprising the step of temporarily latching a logic state indicative of the presence of said first mode and controllably passing said device reset signal to a reset input of said checking ~~means~~ when said logic state is latched.

31. The method of claim 20, further comprising the step of resetting said validity signal upon said device being forced to leave said first mode prematurely.

32. (Currently Amended) The method of claim 20, further comprising the step of controllably inhibiting the transfer of said validity signal to outside said device when said first mode is active.

33. (Currently Amended) The method of claim 20, further comprising the step of delivering to a chip select or chip enable input of said memory means an enable signal when a first mode selection signal, and a protection option signal are active,

34. The method of claim 33, further comprising the step of delivering said enable signal on the further condition that an address belonging to said memory means has been selected at an address input thereof.

35. The method of claim 20, wherein said protected data comprises program code.

36. (Currently Amended) The method of claim ~~1~~20, implemented in a microcontroller unit or microprocessor chip.